Vivekanand Education Society's

Department of Electronics & Telecommunication Engineering

(Autonomous Institute Affiliated to University of Mumbai, Approved by AICTE)

Department of Electronics & Telecommunication Engineering

VLSI & Embedded System Design

ME, Semester I-IV

AY: 2023-24

Semester I

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
VEC101	VLSI design	3	1	--	3	1	--	4
VEC102	Designing with ARM cortex Processor	3	1	--	3	1	--	4
VEPE101X	Program Elective 1	3	1	--	3	1	--	4
VEPE102X	Program Elective 2	3	1	--	3	1	--	4
VEEL101	Skill Based Lab- I	--	4$	--	--	2	--	2
Total		**12**	**06**	**--**	**12**	**06**	**--**	**18**

Course Code	Course Name	Examination Scheme							
		Theory					Term Work	Pract /Oral	Total
		Internal Assessment			End Sem. Exam	Exam. Duration (in Hrs)			
		Mid Term	CA	Total					
VEC101	VLSI design	20	20	40	60	2	25	--	125
VEC102	Designing with ARM cortex Processor	20	20	40	60	2	25	--	125
VEPE101X	Program Elective 1	20	20	40	60	2	25	--	125
VEPE102X	Program Elective 2	20	20	40	60	2	25	--	125
VEEL101	Skill Based Lab- I : Verilog Programming	--	--	--	--	--	50	50	100
Total		**--**	**--**	**160**	**240**	**--**	**150**	**50**	**600**

Note 1:

1. $ indicates work load of Learner (Not Faculty), for Skill Based Lab
2. Each Faculty to designate lab related work for individual subjects as per syllabus.
3. Skill Based Lab- I will be based on Verilog.

 # Program Elective

Every student is required to take one Program Elective Course for Semester I and Semester II. Different sets of courses will run in both the semesters. Students can take these courses from the list of program electives, which are closely allied to their disciplines.

SEMESTER I			
Elective 1		**Elective 2**	
Course Code	**Program Elective (PE)**	**Course Code**	**Program Elective (PE)**
VEPE1011	RF Microelectronics	VEPE1021	Hardware software co-design
VEPE1012	Computer organization and Reconfigurable computing	VEPE1022	RTOS & Embedded Linux
VEPE1013	Electronics System Design	VEPE1023	Software for embedded systems
VEPE1014	Architectural design of Digital Integrated Circuits	VEPE1024	SoC Design

Semester II

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
VEC201	Analog Mixed signal VLSI	3	1	--	3	1	--	4
VEC202	Advance verification techniques using System VERILOG	3	1	--	3	1	--	4
VEPE201X	Program Elective-3	3	1	--	3	1	--	4
VEPE202X	Program Elective-4	3	1	--	3	1	--	4
VEEL201	Skill Based Lab-II: Python & TCL	-	4$	--	--	2	--	2
Total		**12**	**06**	**--**	**12**	**06**	**--**	**18**

Course Code	Course Name	Examination Scheme							
		Theory					Term Work	Pract /Oral	Total
		Internal Assessment			End Sem. Exam	Exam. Duration (in Hrs)			
		Mid Term	CA	Total					
VEC201	Analog Mixed signal VLSI	20	20	40	60	2	25	--	125
VEC202	Advance verification techniques using System VERILOG	20	20	40	60	2	25	--	125
VEPE201X	Program Elective-3	20	20	40	60	2	25	--	125
VEPE202X	Program Elective-4	20	20	40	60	2	25	--	125
VEEL201	Skill Based Lab-II: Python & TCL	--	--	--	--	--	50	50	100
Total		**--**	**--**	**160**	**240**	--	**150**	**50**	**600**

Note 1:

1. $ indicates work load of Learner (Not Faculty), for Skill Based Lab
2. Each Faculty to designate lab related work for individual subject as per syllabus.
3. Skill Based Lab- II shall be based on

 # Program Elective

Every student is required to take one Program Elective Course for Semester I and Semester II. Different sets of courses will run in both the semesters. Students can take these courses from the list of program electives, which are closely allied to their disciplines.

SEMESTER II			
Elective 1		**Elective 2**	
Course Code	**Program Elective (PE)**	**Course Code**	**Program Elective (PE)**
VEPE2011	Real time systems	VEPE2021	VLSI architecture for signal processing
VEPE2012	IC fabrication	VEPE2022	Wireless Sensor Network
VEPE2013	Testability of VLSI circuits	VEPE2023	Device drivers
VEPE2014	Communication buses and interfaces design	VEPE2024	Neural networks and Machine learning algorithms

Internal Assessment:

Assessment consists of one Mid Term Test of 20 marks and Continuous Assessment of 20 marks.(Total 40)

Mid Term test is to be conducted when approx. 50% syllabus is completed Duration of the midterm test shall be one hour.

Continuous Assessment:

Continuous Assessment is of 20 marks**.** The rubrics for assessment will be considered on approval by the subject teachers. The rubrics can be any 2 or max 4 of the following:

Sr.no	Rubrics	Marks
1.	*Certificate course for 4 weeks or more: NPTEL/ Coursera/ Udemy/any MOOC	10 marks
2.	Wins in the event/competition/hackathon	10 marks
3.	Content beyond syllabus presentation	10 marks
4.	Creating Proof of concept /case studies	10 marks
5.	Mini Project / Extra Experiments/ Virtual Lab	10 marks
6.	GATE Based Assignment test/Tutorials etc	10 marks
7.	Participation in event/workshop/talk / competition followed by small report and certificate of participation relevant to the subject(in other institutes)	5 marks
8.	Multiple Choice Questions (Quiz)	5 marks

Semester III

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
VEMP301	Major Project: Dissertation -I	--	20	--	--	10	--	10
Total		**00**	**20**	**--**	**00**	**10**	**--**	**10**

Course Code	Course Name	Examination Scheme							
		Theory							
		Internal Assessment			End Sem. Exam	Exam. Duration (in Hrs.)	Term Work	Pract/ Oral	Total
		Mid Term	Test-2	Avg					
VEMP301	Major Project: Dissertation -I	--	--	--	--	--	100	--	100
Total		**--**	**--**	**--**	**--**	--	**100**	**--**	**100**

Online Credit Courses

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut	Theory	Pract	Tut.	Total
VEOCC301	Online Credit Course - I	--	--	--	--	--	--	3
VEOCC301	Online Credit Course - II	--	--	--	--	--	--	3
Total		**--**	**--**	**--**	**00**	**00**	**00**	**06**

Note 1:
It is mandatory to complete the Online Credit Courses (OCC) available on NPTEL / Swayam /MOOC or a similar platform approved by the university. The learner shall opt for one course each from OCC- I and OCC-II. These two courses shall be completed in any semester I or II or III, but not later end of the Semester III. The credits earned with OCC- I and OCC-II shall be accounted in the third semester grade-sheet. The learner shall be allowed to take up these courses from his or her institute or organization/ industry where his / her major project is carried out. The students shall complete the courses and shall qualify the exam conducted by the respective authorities/ instructor from the platform. The fees for any such courses and the corresponding examination shall be borne by the learner. University shall make a provision that credit earned with OCC-I and OCC-II shall be accounted in the third semester grade-sheet with actual names of the courses.

Online Credit Course – I
The learner shall opt for the course in the domain of Research Methodology **or** Research & Publication Ethics or IPR. The opted course shall be of 3 credits of equivalent number of weeks.

Online Credit Course –II
The learner shall opt for the course recommended by Faculty Advisor/ Project Supervisor from the institute. The opted course shall be of 3 credits of equivalent number of weeks.

Semester IV

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
VEMP401	Major Project: Dissertation -II	--	32	--	--	16	--	16
Total		**0**	**32**	**--**	**0**	**16**	**--**	**16**

Course Code	Course Name	Examination Scheme							
		Theory							
		Internal Assessment			End Sem. Exam	Exam. Duration (in Hrs)	Term Work	Prac/ Oral	Total
		Mid Term	Test-2	Avg					
VEMP401	Major Project: Dissertation -II	--	--	--	--	--	100	100	200
Total		**--**	**--**	**--**	**--**	--	**100**	**100**	**200**

Total Credits:68

Note 3: The Dissertation submission shall not be permitted till the learner completes all the credit requirements of ME course.

Semester I

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEC101	VLSI Design	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEC101	VLSI Design	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	Derive the small signal equivalent circuit of the MOSFET and analyze the frequency limitations of the device.
2	To provides an exposure to different methods of VLSI design and the principles behind such design
3	To provides an exposure to RTL design tradeoffs and optimizations

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Analyze CMOS inverter and learn different MOS design styles.
2	Learn to design efficient algorithms and architectures of arithmetic circuits.
3	Able to design RTL.
4	Understand working and design of programmable processors.

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs
1	**MOS Inverter**		5
	1.1	Static Analysis resistive and CMOS inverter: Calculation of all critical voltages and noise margins. Design of symmetric CMOS inverter.	
	1.2	Dynamic Analysis of CMOS inverter: Calculation of rise time, fall time and propagation delay	
2	**MOS Circuit Design Styles**		8
	2.1	Static CMOS, Dynamic CMOS , Pseudo NMOS, Domino, C^2MOS, NORA logic, NP Domino logic, Transmission gate, Pass transistor logic, Mux, charge sharing, charge leakage	
	2.2	Static time analysis :Setup time , Hold time, clock skew, multi-clock, multi-clock domain, MTBF, Latch, D FF,JK FF	
	2.3	Clocked flip-flop, CMOS clock styles, Pipelined systems, Clock generation and distribution,	
3	**Efficient Arithmetic**		8
	3.1	Array Multiplier ,Partial product generation ,reduction ,Wallace multiplier, Booths Multiplier, Booth recoding schemes Conditional Sum Adder, Ling's Adder, Prefix and Parallel prefix adders, Running Average Circuit	
	3.2	Baugh Wooley Multiplier, Architecture of Squaring Circuit, Reconfigurable Constant Multiplier Design, Pipelined Tree and Array Multipliers	
	3.3	Shift/Subtract Division Algorithms, Programmed Division	
4	**FSM Design**		4
	FSM, HLSM, Sum of absolute differences, RTL pitfalls and good practice.		
5	**RTL Design Optimization and trade-offs**		6
	5.1	Pipelining, latency Vs throughput, pipelined FIR filter, concurrency.	
	5.2	**Case Study:** SAD with concurrency, Smaller FIR filter using operator scheduling.	
6	**Programmable Processor Design**		8
	6.1	Single Processor Design.	
	6.2	3-instruction programmable Processor (general purpose processor).	
		Total	**39**

Text Books:

1. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", Tata McGraw Hill, 3rd Edition, 2012.
2. P. Uyemura, "Introduction to VLSi Circuits and Systems", John Wiley and Sons
3. Frank Vahid, ― Digital Design with RTL design, VHDL and VERILOG‖, John Wiley and Sons Publisher 2011

Reference Books:

1. Neil H.E Weste and Kamran Esheaghian "Principles of CMOS VLSI Design" Pearson Education.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", Pearson Education, 2nd Edition.
3. Clive Max Maxfield, The Design Worriors Guide to FPGA Devices, tools and flows, Elsevier.

Assessment: Internal

Assessment Test

Assessment consists of one test on 50% syllabus.

End Semester Examination

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPC102	Designing with ARM Cortex Processor	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPC102	Designing with ARM Cortex Processor	20	20	40	60	25	--	--	125

Course Objectives

Sr. No	The course aims:
1	Study the architecture of ARM series microprocessor and its need in applications
2	Learn architecture and programming for ARM Cortex-M series Microcontroller.
3	Application of RTOS for embedded programming.

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Understand the characteristics and technologies of embedded systems.
2	Describe different program modeling concepts
3	Describe the ARM microprocessor architecture and its features.
4	Understand the functions and programming of various peripherals on ARM.
5	Study the concepts of Real time operating systems and write programs
6	Design embedded systems with available resources.

DETAILED SYLLABUS

Sr No	Topic	Hrs
	Pre-requisites: Microcontrollers, Microprocessor, C-Programming	
1	**Introduction to ARM Cortex** ● History of ARM processors and Series ● ARM Architecture ,Addressing Modes ● Instructions Overview Arithmetic, Logic ,Branch, and Call Instructions ● ARM Memory Map , Memory Access, and Stack ● ARM Pipeline ● Development and debugging Tools for Embedded Systems	8
2	**Cortex M4 Microcontrollers & Peripherals:STM32F401CC** ● Cortex M4-based controller architecture ● ARM Cortex M4 Core, Interconnect Matrix in ARM Cortex M4 Microcontroller ● Reset and Clock Control, Clock Recovery System, Power Control ● Memory mapping, ● Cortex M4 Peripherals – RCC, GPIO, Timer, System timer, PWM	7
3	**Cortex M4 Microcontrollers & Peripherals:STM32F401CC** ● Cortex M4 Peripherals -- ADC,RTC ● DMA Interfacing ● LCD Interfacing ● OLED Graphics Display Interfacing	6
4	**Embedded Communication Protocols** ● UART (RS485) ● SPI, I2C ● USB ● Canbus	6
5	**Memory, Safety and Security in ARM Cortex Microcontroller** ● Flash, Quad SPI Interface, Flexible Memory controller ● CRC, Random Number Generator, memory protections,MMU ● Advanced Encryption Standard HW Accelerator (AES), Safety support	6
6	**Advanced Embedded Controllers, Features and case studies** ● Programming for Power-Efficient Computing - High Level and low ● level Techniques ● Cortex M7, M23 and M33 Controllers and Features ● Embedded Systems case studies - Consumer, Medical, Automotive	6

Textbooks:

1. ARM assembly Language programming and Architecture Muhammed Ali Mazidi ,Sarmad Naimi,Sepehr Naimi and Shuejn Chen by Microdigital Ed
2. Beginning STM32 Warren Gay apress Publication
3. Shibu K.V," Introduction to Embedded Systems", Mc Graw Hill, 2nd edition.
4. Frank Vahid, and Tony Givargis, "Embedded System Design: A unified Hardware/Software Introduction", Wiley Publication.
5. Raj Kamal," Embedded Systems Architecture, Programming and design",Tata MCgraw-Hill Publication.

6. Dr. K.V.K.K. Prasad, “Embedded Real Time Systems: Concepts, Design & Programming”,Dreamtech Publication.
7. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M”, Newness, ELSEVIER.
8. ARM Systems Developer’s Guides- – A. N. Sloss, D. Symes, C. Wright, Elsevier 2008.
9. Embedded Microcomputer Systems, Real Time Interfacing – J.W. Valvano, Cole, 1999.

Internal Assessment:
Assessment consists of one Mid Term Test of 20 marks and Continuous Assessment of 20 marks. Mid Term test is to be conducted when approx. 50% syllabus is completed Duration of the midterm test shall be one hour.

End Semester Examination:
Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examination.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE1011	RF Microelectronics	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE1011	RF Microelectronics	20	20	40	60	25	--	--	125

Course Objectives

Sr. No	The course aims:
1	To understand RF microelectronics
2	To model RF devices using semiconductors

Course Outcomes

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Understand the behavior of RF passive components and model active components.
2	Perform RF amplifier design
3	Design RF oscillators
4	Model RF semiconductor based devices

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs
1	**Module 1**		5
		Introduction; application of RF electronics in modern systems;	
2	**Module 2**		8
		basic concepts in RF circuit design, active RF components: various RF diodes and transistors and their circuit models, matching and biasing networks,	
3	**Module 3**		8
		RF amplifier design: low power, low noise and broadband amplifiers	
4	**Module 4**		4
		RF oscillator design; negative resistance oscillator; dielectric resonator oscillators, phase noise.	
5	**Module 5**		6
		RF Mixers: Balanced mixers; low noise mixers; noise in RF circuits, microwave transmitters and receivers	
6	**Module 6**		8
		Microwave Semiconductor Devices And Modelling: PIN diode, Tunnel diodes, varactor diode, schottky diode, IMPATT and TRAPATT devices, transferred electron devices, Microwave BJTs, GaAs FETs, low noise and power GaAs FETs, MESFET, MOSFET and HEMT.	
		Total	**39**

Text Books:

Assessment: Internal
Assessment Test:
Assessment consists of one test on 50% syllabus.

End Semester Examination:
Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examination.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical /Oral	Tutorial	Total
VEPE1012	Computer architecture and Reconfigurable computing	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE1012	Computer architecture and Reconfigurable computing	20	20	40	60	25	--	--	125

Course Objectives

Sr. No	The course aims:
1	To provide broad and deep knowledge of computer architecture issues and techniques.
2	Understand CISC & CISC processor
3	Knowledge of RISC processor

Course Outcomes:

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Understand Instruction Level implementation of RISC Hardware level.
2	Understand instruction level Hazards.
3	Understand architecture of FPGA
4	Know the of FPGA flow
5	Understand reconfigurable algorithms and techniques.
6	Understand Instruction Level implementation of RISC Hardware level.

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs
1	**CISC**		5
		Overview of CISC processor architectures; Instruction set architecture of CISC processor;	
2	**RISC Processor**		8
		RISC instruction set architecture (MIPS); Building a Data path, Pipelined execution of RISC instructions;	
3	**Pipeline and hazards**		8
		Pipeline execution unit design; data hazard, control hazards.	
4	**FPGA Architecture**		4
		Overview of Programmable Logics. FPGA fabric architectures. Logic Elements and Switch.	
5	**FPGA Design Flow**		6
		Networks. Design and Synthesis of Combinational and Sequential Elements. Placement and Routing. Pipelining and other Design Methodologies. Fine-grained and Coarse-Grained FPGAs	
6	**Reconfigurable computing**		8
		Static and Dynamic Reconfiguration. Partitioning. Hardware/Software Portioning and Partial Evaluation. Systolic Architectures.	
			39

Text Books:

1. Computer Organization and Design- The Hardware Software Interface:4th Edition. Author: John L. Hennessy & David A. Patterson Publisher: Morgan Kaufmann, Year: 2011
2. Clive Max Maxfield, The Design Worriors Guide to FPGA Devices, tools and flows, Elsevier.
3. J.P. Hayes, Computer Architecture and Organization, McGraw Hill.

Assessment: Internal

Assessment Test:

Assessment consists of one test on 50% syllabus.

End Semester Examination:

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examination.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE1013	Electronic Systems Design	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE1013	Electronic Systems Design	20	20	40	60	25	--	--	125

Course Objectives

Sr. No	The course aims
1	To provide students with knowledge to design basic electronic systems.
2	To make students aware of practical design considerations like noise reduction, grounding techniques, shielding and isolation which are required to design high performance electronic instrumentation systems.

Course Outcomes

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Design linear integrated circuits and their applications
2	Design advanced circuits of Instrumentation amplifier
3	Implement non-linear circuits for various signal processing applications.
4	Evaluate the performance of different A/D conversion techniques
5	Develop system which is able to reject noise pick up
6	learn the power management challenges in low power portable systems design

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
1	**Design of linear integrated circuits and their applications**		6
		Linear and log amplifiers, peak detect and milli volt rectifier circuits, analog switches and multiplexers, current and voltages references and their stability	
2	**Instrumentation and special operational amplifiers**		7
		Advanced instrumentation amplifier and various designs to improve dynamic range and reduce power dissipation. High speed OP-amps CMOS OP-amps Micro power amplifiers low noise and chopper stabilized OP-amps	
3	**Nonlinear integrated circuits**		8
		Comparators, voltage to frequency and frequency to voltage converters switched capacitor circuit‘s filters. Analog filters, Sample and hold circuits.	
4	**Converters**		10
		D.C to D.C converters. Mixed signal processing. High speed and high resolution DACs and A/D converters. Various techniques of A/D conversion. Flash, successive approximation, multi slope ADC. Delta sigma ADC.	
5	**Noise reduction techniques**		4
		Design of mixed signal processing circuits, grounding and isolation techniques R.F shielding, Power supply noise reduction and filtering, Over voltage and ESD protection.	
6	**Power Management**		4
		Power management issues in low power portable systems, Linear and switch mode regulators.	
			39

Text Books:

1. E.Allen Douglas R.Holberg, ―CMOS Analog Circuit Design‖, Philip Oxford , University Press 2004
2. Kevin M.Daugherty, ―Analog To Digital Converter‖, Tata McGraw Hill Inc 1995
3. Manual: High Speed Design Technique- Analog Devices Inc 1996
4. Dan Shiengold, ―Non Linear Integrated Circuits Hand Book‖, Analog Devices.
5. Ralph Morrison,‖Grounding And Shielding Technique‖, Fourth Edition,John Wiley,1998

Internal Assessment:

Assessment Test:

Assessment consists of one test on 50% syllabus.

End Semester Examination:

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examination.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical /Oral	Tutorial	Total
VEPE1014	Architectural design of Digital Integrated Circuits	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE1014	Architectural Design of Digital Integrated Circuits	20	20	40	60	25	--	--	125

Course Objectives

Sr. No	The course aims:
1	To describe the characteristics of computationally intensive algorithms
2	To identify the bottlenecks of intensive computations.
3	To learn various techniques to map Arithmetic and machine learning algorithms on hardware to improve performance.

Course Outcomes:

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Design and analyze sequential circuits using FSMs
2	Explain various typical Arithmetic algorithms and their applications
3	Describe various methodologies/techniques to map DSP algorithms on Hardware
4	Analyze various hardware architectures available to implementation DSP algorithms
5	Evaluate and select efficient fault tolerant architectures.
6	Design/propose hardware architecture for effective implementation of machine learning algorithms on hardware

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
1	**FSM**		5
		FSM, Analysis and synthesis of FSM, State reduction, Asynchronous FSM: Designing, cycles and races, hazards-static, dynamic and essential Hazards.	
2	**Efficient Algorithm to Architecture Mapping**		8
	2.1	Design of N-bit incrementer, decrementer, complimenter, Cogustone Multiplier.	
	2.2	Techniques to enhance circuit performance, pipelining and parallel processing, circuit design for N bit natural numbers, optimized circuit design for different functions.	
	2.3	Floating Point Arithmetic : Adders/subtractors, Multipier, Divider	
3	**Fault Tolerant Arithmetic**		6
	3.1	Faults, Errors, and Error Codes.	
	3.2	Arithmetic Error-Detecting Codes, Arithmetic Error-Correcting Codes.	
	3.3	Self-Checking Function Units, algorithm-based fault tolerance.	
4	**High Throughput Arithmetic**		6
	4.1	High throughput Arithmetic : pipelined arithmetic functions, clock rate and throughput	
	4.2	Systolic Arithmetic inputs	
5	**DSP Architectures**		8
	5.1	Design of fixed point, floating point arithmetic units,	
	5.2	MAC and SOP, CORDIC architectures	
	5.3	FFT Architecture	
6	**Efficient Design of Machine Learning Hardware**		6
	6.1	Artificial Intelligence and Machine Learning, Software and Co-design Optimizations,Pruning, Systolic array convolution	
		Total	**39**

Textbooks

1. VLSI Digital Signal Processing Systems Design and Implementation – Khesab Parhi
2. COMPUTER ARITHMETIC Algorithms and Hardware Designs-Behrooz Parhami
3. Machine Learning in VLSI-Ibrahim (Abe) M. Elfadel, Duane S. Boning, Xin Li, Computer-Aided Design

Reference Books

1. Bill Franks, ―Taming The Big Data Tidal Wave: Finding Opportunities in Huge Data Streams with Advanced Analytics‖, Wiley
2. Chuck Lam, ―Hadoop in Action‖, Dreamtech Press

E-Resources

1. https://nptel.ac.in/courses/108105118
2. https://nptel.ac.in/courses/108106149
3. https://nptel.ac.in/courses/108105157

Internal Assessment:

Assessment Test:

Assessment consists of one test on 50% syllabus.

End Semester Examination:

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examination.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical /Oral	Tutorial	Total
VEPE1021	Hardware software co-design	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE1021	Hardware software co-design	20	20	40	60	25	--	--	125

Course Objectives

Sr. No	The course aims:
1	
2	
3	
4	
5	
6	

Course Outcomes:

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	
2	
3	
4	
5	
6	

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
1	**Module 1**		5
		FPGA and ASIC based design	
2	**Module 2**		8
		Low-Power Techniques in RT Embedded Systems On-chip networking	
3	**Module 3**		8
		Hardware Software partitioning and scheduling,	
4	**Module 4**		4
		Co-simulation, synthesis and verifications	
5	**Module 5**		6
		Architecture mapping	
6	**Module 6**		8
		HW-SW Interfaces and Re-configurable computing.	
		Total	39

Text Books:

References Books:

Internal Assessment:
Assessment Test:
Assessment consists of one test on 50% syllabus.

End Semester Examination:
Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examination.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical /Oral	Tutorial	Total
VEPE1022	RTOS & Embedded Linux	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE1022	RTOS & Embedded Linux	20	20	40	60	25	--	--	125

Course Outcomes:

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Learn about the basics of real-time concepts
2	Incorporate RTOS in an Embedded system.
3	Get knowledge in Embedded OS (Linux) fundamentals
4	Comprehend Embedded Processor and its software
5	Comprehend the booting process of Embedded Linux Systems
6	Comprehend the configuration of Embedded Linux Drivers

DETAILED SYLLABUS

Sr. No	Topic	Hrs
1	**MODELLING WITH HARDWARE/SOFTWARE DESIGN APPROACHES** • Modelling embedded systems- • Embedded software development approach • Overview of UML modeling with UML • UML Diagrams-- Hardware/Software Partitioning • Co-Design Approaches for System Specification and modeling	4
2	**System architecture of FreeRTOS** • Introduction FreeRTOS, • Thread Creation and Management, • Thread Synchronization Mechanisms, • IPC – RTFIFO, Shared Memory, Interrupt Handling • Inter Task Communication Mechanisms, • Semaphores, Message Queues, Pipes, • Interrupts	9
3	**Introduction** • Basic Operating System Concepts • History& Benefits of Linux • Fundamentals of Embedded Linux OS • Comparison of Embedded OS • Embedded OS Tools and IDE • Embedded Linux Applications and Products.	5

4	**The architecture of Embedded Linux:**
	• What is Kernel?
	• Task of kernels
	• Types of kernels
	• Kernel Architecture Overview
	  o User Space
	  o Kernel Space
	• Kernel Functional Overview
	  o File System
	  o Process Management
	  o Address Spaces and Privilege Levels
	  o Memory Management
	  o System Calls
	  o Inter Process Communication (IPC) – Pipes, FIFo & Shared Memory
	  o Device Drivers
	  o Network
		9

5	**Linux Bootloader & U-Boot:** • Boot-loader Phases • U-boot – Embedded boot loader • What does u-boot do? • Navigating the u-boot sources	7
6	**Configuring the Linux Environment:** • Linux environment • Types of Hosts • Types of Host/Target Development Setups	5

	• Types of Host/Target Debug Setups • Embedded Environment Tools **Tool-chain: Configuration and Cross-Compilation:** • What is a tool-chain? • Native vs. cross-compilation • Toolchain Components • Toolchain choices	

Reference Books

1. GNU/LINUX Application Programming, Jones, M Tims
2. Sreekrishnan Venkateswaran Essential Linux Device Drivers, Prentice Hall 2008
3. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK
4. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17th IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society
5. Free RTOS Reference Manual

Assessment: Internal

Assessment Test:

Assessment consists of one test on 50% syllabus.

End Semester Examination:

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examinations.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical /Oral	Tutorial	Total
VEPE1023	Software for embedded systems	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE1023	Software for embedded systems	20	20	40	60	25	--	--	125

Course Objectives

Sr. No	The course aims:
1	To understand various satellite communication techniques
2	Know about satellite systems

Course Outcomes

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Visualize the architecture of satellite systems as a means of high speed, high range communication system.
2	State various aspects related to satellite systems such as orbital equations, sub-systems in a satellite, link budget, modulation and multiple access schemes.
3	Solve numerical problems related to orbital motion and design of link budget for the given parameters and conditions.

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
		Pre-requisites: Embedded system, microcontrollers, ARM	
1	**Module 1**		5
		Real-time and embedded systems; software issues in embedded system; software development process;	
2	**Module 2**		8
		requirement analysis: use cases, identification and analysis of use cases, use case diagrams;	
3	**Module 3**		8
		design: architectural design, design patterns and detailed design;	
4	**Module 4**		4
		implementation: languages, compilers, runtime environments and operating systems for embedded software, Testing methodology	
5	**Module 5**		6
		Object Oriented Programming with Embedded C++: - Differences between C and C++, Fundamentals of object oriented programming; OOP vs. Procedure oriented programming. - OOP concepts: classes, objects, abstraction, polymorphism, inheritance, data binding and encapsulation. -	
6	**Module 6**		8
		Basics of C++: features of C++, data types, standard I/O, arrays and strings in C++. - Classes in C++, instantiation, creating objects and object scope, data abstraction, data encapsulation, constructors and destructors, methods and access modifiers, function and operator overloading - Inheritance-Base and Derived classes, Inheritance types, Scope Resolution operator; polymorphism and virtual functions, exception handling	
			39

Text Books:

1. Michael J. Pont , “Embedded C”, Pearson Education, 2nd Edition, 2008
2. Martin C. Brown,” Python: The Complete Reference”, McGraw-Hill Education, 2001
3. A. Michael Berman, “Data structures via C++”, Oxford University Press, 2002
4. Robert Sedgewick, “Algorithms in C++”, Addison Wesley Publishing Company, 1999
5. Abraham Silberschatz, Peter B, Greg Gagne, “Operating System Concepts”, John Willey & Sons, 2005
6. E. Balaguruswami, “Object-Oriented Programming With C++”, McGraw-Hill Education, 7 th Edition, 2017

Internal Assessment: Assessment Test:

Assessment consists of one test on 50% syllabus.

End Semester Examination:

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examination.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical /Oral	Tutorial	Total
VEPE1024	SoC Design	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE1024	SoC Design	20	20	40	60	25	--	--	125

Course Objectives

Sr. No	The course aims:
1	To introduce modern system design using SoC
2	To understand the concept of hardware software co-design
3	To learn software and hardware design integration

Course Outcomes

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Design SoC based system for engineering applications.
2	Design and verify SoC system
3	Analyze routing issues in SoC Design
4	Interpret complex SoC design issues
5	Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development
6	Identify and formulate a given problem in the framework of SoC based design approaches.

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
		Pre-requisites: Digital System Design, Advanced VLSI, Embedded system	
1	**Module 1**		5
		ASIC - Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific, Instruction Processor (ASIP) concepts.	
2	**Module 2**		8
		NISC - NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.	
3	**Module 3**		8
		Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues	
4	**Module 4**		4
		Verification technology options, Verification methodology. System level verification, block-level verification. Timing verification	
5	**Module 5**		6
		Synthesis - Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs.	
6	**Module 6**		8
		Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization	
			39

Text Books:

1. Engineering the Complex SOC: Fast, Flexible Design with Configurable Processors-Chris Rowen, Pesrson, 2004.
2. System on a chip verification: Methodology and Verification-Second edition, Prakash Rashinkar, Peter Paterson, Leena Singh, Kluwer Academic Publishers
3. System-on-a-Chip: Design and Test- Rochit Rajsuman-Artech house-2002
4. VLSI Physical design Automation: Theory and Practice, Sadiq Sait, Habib Youssef, World Scientific Publishing, 1999
5. Surviving the SoC revolution- Henry Chang, Larry Cooke, Grant Martin, Kluwer Academic Publishers-2002
6. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006.
7. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

Internal Assessment:

Assessment Test:

Assessment consists of one test on 50% syllabus.

End Semester Examination:

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, out of these any four questions to be attempted by students. Minimum 80% syllabus should be covered in question papers of end semester examination.

Semester II

Course Code	Course Name	Teaching Scheme(Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
VEC201	Analog Mixed signal VLSI	3	1	--	3	1	--	4
VEC202	Advance verification techniques using System Verilog	3	1	--	3	1	--	4
VEPE201X	Program Elective-3	3	1	--	3	1	--	4
VEPE202X	Program Elective-4	3	1	--	3	1	--	4
VEEL201	Skill Based Lab-II: Python & TCL	- -	4$	--	--	2	--	2
Total		**12**	**06**	**--**	**12**	**06**	**--**	**18**

Course Code	Course Name	Examination Scheme							
		Theory					Term Work	Pract / Oral	Total
		Internal Assessment			End Sem. Exam	Exam. Duration (in Hrs)			
		Test	CA	Total					
VEC201	Analog Mixed signal VLSI	20	20	40	60	3	25	--	125
VEC202	Advance Verification Techniques using System Verilog	20	20	40	60	3	25	--	125
VEPE201X	Program Elective-3	20	20	40	60	3	25	--	125
VEPE202X	Program Elective-4	20	20	40	60	3	25	--	125
VEEL201	Skill Based Lab-II: Python & TCL	--	--	--	--	--	50	50	100
Total		**--**	**--**	**160**	**240**	--	**150**	**50**	**600**

Note

1) $ indicates work load of Learner (Not Faculty), for Skill Based Lab
2) Each Faculty to designate lab related work for individual subject as per syllabus.
3) Skill Based Lab- II shall be based on Python & TCL.

 # Program Elective

Every student is required to take one Program Elective Course for Semester I and Semester II. Different sets of courses will run in both the semesters. Students can take these courses from the list of program electives, which are closely allied to their disciplines.

SEMESTER II			
Program Elective 3		**Program Elective 4**	
Course Code	**Program Elective (PE)**	**Course Code**	**Program Elective (PE)**
VEPE2011	Real time systems	VEPE2021	VLSI Architecture for Signal Processing
VEPE2012	IC fabrication	VEPE2022	Wireless Sensor Network
VEPE2013	Testability of VLSI circuits	VEPE2023	Device Drivers
VEPE2014	Communication Buses and Interfaces Design	VEPE2024	Neural Networks and Machine Learning Algorithms

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEC201	Analog Mixed signal VLSI	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEC201	Analog Mixed signal VLSI	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	To understand basics of analog devices, fabrication and layout
2	To explain different configurations of single stage amplifiers and their frequency response.
3	To describe and analyze current mirrors.
4	To represent noise in various analog circuits and its effects and removal techniques.
5	To analyze and design OP-AMPs and other analog and mixed signal blocks and band gap references.

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Design layout of analog as well as digital circuits
2	Design basic building blocks like current/voltage sources and basic gain stages.
3	Learn advanced analog circuits such as cascaded stages, cascade, and differential amplifiers.
4	Design OPAMPs, Band gap reference circuits
5	Analyze noise and frequency of analog devices
6	Design mixed signal circuits such as ADC, DAC, Sigma-Delta Converters, PLL/DLL

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
		Pre-requisite: Advanced VLSI design, Microelectronics	
1	**MOS Fundamentals**		5
		MOS fabrication, CMOS fabrication, Layout design rules, Stick Diagrams, Layouts of different devices.	
2	**Current Mirrors**		4
	2.1	Passive and active current mirrors, basic current mirrors, cascode current mirrors,	
	2.2	Active current mirrors, large and small signal analysis, common mode properties.	
3	**Amplifiers**		8
	3.1	Common source, source follower, common gate, cascade, folded cascode	
	3.2	Basic differential pair, common mode response, single ended differential operation, differential pair with MOS loads, frequency response of all amplifiers, association of poles with nodes.	
4	**Noise and Feedback**		6
		Representation of noise in circuits, noise in single stage amplifiers and cascade stages, noise in differential pairs, noise bandwidth, general feedback considerations, feedback topologies, effect of loading, effect of feedback on noise.	
5	**Operational amplifiers**		8
	5.1	One stage and two stage op amps, gain boosting, common mode feedback, input range limitation, slew rate, power supply rejection, noise in op-amp, stability and frequency compensation, multi pole system, phase margin, frequency compensation, compensation of two stage op-amps, other compensation techniques, two stage comparator	
6	**Data converter fundamentals and architecture**		8
	6.1	Oscillators: General considerations, Ring oscillators, LC oscillators, VCO	
	6.2	Phase-Locked Loop: Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications of PLL in integrated circuits	
	6.3	DAC architectures: Digital input code, resistors string, R-2R ladder networks, current steering, charge scaling DACs, Cyclic DAC, pipeline DAC ADC architectures: Flash, Two Step Flash, Pipeline ADC, Integrating ADCs, Successive approximation ADCs	
		Total	**39**

Text Books:

1. Behzad Razavi, Design of Analog CMOS integrated circuits, Tata McGraw Hill Edition, 2002
2. Philip E Allen, Douglas R. Holberg, CMOS Analog Circuit Design, Oxford, 2002
3. David A Johns, Ken Martin, Analog Integrated Circuit Design, Wiley Students edition, 2002
4. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog Integrated Circuits", Willey, 5 th Edition
5. Neil H. E. Weste, David Harris and Ayan Banerjee, ―CMOS VLSI Design: A Circuits and Systems Perspective‖, Pearson Education, 3rd Edition.

Reference Books:

1. Neil H.E Weste and Kamran Esheaghian "Principles of CMOS VLSI Design" Pearson Education.
2. R. Jacaob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, Student Edition

Assessment: Internal
Assessment Test
Assessment consists of one test on 50% syllabus.

End Semester Examination
Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical /Oral	Tutorial	Total
VEC202	Advance verification techniques using System VERILOG	03	--	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEC202	Advance verification techniques using System VERILOG	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	Discuss fundamental System Verilog concepts of today's most advanced digital design techniques.
2	Offers broad coverage of System Verilog HDL from a verification perspective.
3	Explains timing and delay simulation; and introduces many other essential techniques for creating tomorrow's complex digital designs.

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Able to apply the Simulation and Synthesis of Digital Circuits.
2	To design Test benches.
3	Able to explain the System Modeling with Tasks and Functions.
4	Create Functional coverage using system Verilog
5	Create Test environment using UVM
6	Create verification flow using system Verilog

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
		Pre-requisite: Digital system design, Verilog Lab-1	
1	**Verification**		4
		Advanced Test bench Structures and Evolution of verification techniques. Role of re-use in verification. Verification stages in ASIC design flow, understanding sign off criteria for verification. Transaction level modeling (TLM): Fundamentals of TLM	
2	**System Verilog Basics of SV**		8
		User defined types, Enumeration, Casting, Parameterized types Dynamic Arrays, Associative Arrays, Queues/Lists, Structures System Verilog Scheduler, Program Control, structures, Packages, Tasks & Functions, Dynamic Processes Control Interposes Sync & Communication, Semaphore, mailbox.	
3	**Classes**		8
	3.1	Constructors, Inheritance, Virtual methods, Protection, Parameterized classes, Polymorphism, Virtual Classes Interfaces: Interface, Virtual Interfaces. Randomization& Constraints: Stimulus Generation techniques, Constraint blocks, Randomize, Random sequences.	
4	**Functional Coverage**		6
	4.1	Cover group, Cover point, Cross Coverage methods.SV-Assertions: Immediate assertions, Concurrent assertions, Boolean Expressions, Sequences, Property Block, Verification Directives, Local Data values.	
	4.2	DPI: Matlab-SV integration, C models to SV integration	
5	**UVM**		8
	5.1	UVM Transactions, Core Utility Functions and Implementation UVM Components, Phases, Creating Components & Running the Simulation, Factory, Starting the Test, Ending the Test, Connection to the DUT Transactions, Configuration, UVM Resources and config_db. Introduction to Sequences: Sequence Elements, Sequences, Sequencers, Drivers to Sequencer to sequence Connection, Virtual Sequences, Prioritized Item Selection and Arbitration.	
6	**VERIFICATION PLAN Switch** (packet based protocol)		5
		Specification, Feature extraction, Stimulation Generation Plan, Coverage Plan, Verification Environment, Scoreboard	
		Total	**39**

Text Books:

1. System Verilog Assertions by Srikanth Vijayaraghavan, Meyyappan Ramanathan Publisher: Springer.
2. IEEE 1800-2012 SV LRM.
3. Getting Started with UVM: A Beginner's Guide Kindle Editionby Vanessa R. Cooper.
4. Doulos UVM Golden Reference Guide Kindle Editionby John Aynsley, David Long, Doug Smith.
5. System Verilog for Design Second Edition: A Guide to Using System Verilog for Hardware Design and Modelling Hardcover by P. Moorby, Stuart Sutherland, Simon Davidmann.
6. System Verilog for Verification: A Guide to Learning the Test Bench Language Featuresby Chris Spear, Greg Tumbush.
7. IEEE 1666-2011.https://verificationacademy.com/
8. http://testbench.in/

Assessment: Internal

Assessment Test

Assessment consists of one test on 50% syllabus.

End Semester Examination

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE2011	Real time systems	03	02	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE2011	Real time systems	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	To make the students aware of the need of real time systems.
2	To understand basic issues for real time OS issues.
3	To study uCOS-II as a case study of RTOS.
4	To acquire skill of using uCOS.
5	To make students aware of the embedded Linux operating system.

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Identify need of Real Time Systems.
2	Able to port uCOS-II operating system on ARM7/AMR Cortex M3 Board.
3	Able to complete 5 programs in uCOS-II on ARM7/Cortex M3.
4	Understand ARM9 architecture and Linux as in embedded hardware.
5	To install Linux and use bootloader and Complete at least 5 assignments based of programming the embedded Linux.

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
		Pre-requisite: Embedded system, microcontrollers, ARM	
1	**Module 1**		5
		Real Time Systems Concepts: Real Time Systems, Characteristics, Hard and Soft Real Time Systems, Critical section of code, Resource, Shared resource, multitasking, Task, Context switch, Kernel, Scheduler, Dispatcher, Preemptive Kernel, Non-Preemptive Kernel, Reentrancy, Round robin, scheduling, Task Priorities, Static & Dynamic Priority, Priority Inversion, Assigning task priorities, Mutual Exclusion, Deadlock, Clock Tick, Memory requirements, Advantages & disadvantages of real time kernels.	
2	**Module 2**		8
		µCOS II: History and Definition of RTOS, Key Characteristics of RTOS, Features of µCOS II, Kernel structure, µCOS II RTOS services: Task management: Tasks, Task states and Control block, Task scheduling, task level context, switching, Idle task, Time management: Clock Tick, Implementing delay in RTOS, resuming the delayed task, getting system time, Placing task in ECB, wait list, Removing a task from ECB, List of Free ECBs, Initializing an ECB, Making a Task Ready, and wait for and event. Implementing timeout in RTOS.	
3	**Module 3**		8
		Inter-Task Communication and Synchronization: Semaphore, Creating/deleting a Semaphore, Waiting, signaling semaphore, Mutex, Creating/deleting and handling Mutex, Event flag, management, Timer Interrupt Service Routines (ISR), Soft Timers, Mail box, sending / getting a message using mailbox as semaphore, message queue and its management, Memory control block. Case studies of uCOS based applications.	
4	**Module 4**		4
		Embedded Linux Development Environment: Need of Linux, Embedded Linux Today, Open source and the GPL, BIOS and Boot loader, Anatomy of an Embedded System, Storage Considerations, Embedded Linux Distributions, Processors for embedded Linux stand alone and integrated processors, ARM9 architecture and ARM9 based processors. ARM flavors and features of various chipsets/architectures, Anatomy of embedded Linux setup, Booting and Initialization of Kernel. Storage considerations, Flash file systems, Execution contexts, Commercial embedded Linux distributions, Embedded Development Environment, Cross-Development Environment, Development Tools, GNU Debugger, Tracing and Profiling Tools, Binary Utilities, Overview of Commands, File I/O (open, create, close, seek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).	
5	**Module 5**		6
		Linux Kernel Construction: Linux Kernel Background, Linux Kernel Construction, Kernel Build System, Kernel Configuration, Role of a Bootloader, Bootloader Challenges. A Universal Bootloader: Das Boot, Porting U-Boot, Device Driver Concepts, Module Utilities, Driver Methods, Linux File System & Concepts.	
6	**Module 6**		8
		Embedded Software Development, Testing Process and Tools: Embedded Software Development process and tools, Host and Target Machines, Target System Tools and Image transfer, Embedded Loader, Monitor, linking and Locating Software, Getting Embedded Software into the Target System, Issues in Hardware- Software Design and Co-design. Testing on Host Machine, Simulators, Laboratory Tools, Case study of embedded system like Automatic Chocolate Vending Machine, Mobile Phone.	
		Total	**39**

Text Books:

1. MicroC OS II: The Real Time Kernel Jean J. Labrosse CMP books.
2. Real-Time Concepts for Embedded Systems Qing Li, Caroline Yao Elsevier.
3. Simple Real-time Operating System: A Kernel, ChowdaryVenkateswara, Amazon.
4. Christopher Hallinan, "Embedded Linux Primer -A Practical, Real-World Approach"2nd ed., Prentice Hall.
5. Building Embedded Linux Systems, KarimYaghmour, Jon Masters, Gilad Ben-Yossef, Philippe Gerum, O'Reilly Media; Second Edition edition (August 22, 2008).
6. Embedded Linux System Design and Development b P Raghvan, Amol Lad, SriramNeelakandan,
7. Auerbach Publications.
8. Advanced UNIX Programming, Richard Stevens.

Assessment: Internal

Assessment Test

Assessment consists of one test on 50% syllabus.

End Semester Examination

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE2012	IC fabrication	03	02	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE2012	IC fabrication	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	To teach fundamental principles of fabrication of VLSI devices and circuits.
2	To provide knowledge about novel VLSI devices.

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.
2	Demonstrate a clear understanding of various MOS fabrication processes, semiconductor measurements, packaging, testing and advanced semiconductor technologies.
3	Discuss physical mechanism in novel devices.
4	Verify processes and device characteristics via simulations.

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
		Pre-requisite: Digital system design, Microelectronics	
1	**Module 1**		5
		Crystal growth, wafer fabrication, and basic properties of Silicon wafers, crystal structure and growth methods, crystal defects, Wafer cleaning, clean room concepts.	
2	**Module 2**		8
		Lithography, optical, deep UV techniques, photo resist, exposure and development, E-beam lithography, X-ray lithography.	
3	**Module 3**		8
		Thermal oxidation and Si-SiO2 interface, manufacturing methods – dry and wet oxidation, thin and thick film oxide growth kinetics, models of oxidation kinetics, polysilicon oxidation, silicide oxidation, Si-SiO2 interface charge	
4	**Module 4**		4
		Dopant diffusion, measurement methods, models and simulation, ion implantation, models and simulation, Thin film deposition- manufacturing methods, measurement methods, models and simulation.	
5	**Module 5**		6
		Etching- manufacturing methods, measurement methods, models and simulation, Wet chemical etching, dry physical etching, dry chemical etching, reactive ion etching, ion beam techniques Device Isolation, Contacts and Metallization, CMOS Design flow N-well , P-well, Twin tub process, Measurements, Packaging and Testing of IC.	
6	**Module 6**		8
		Novel devices: Nanowire -Fabrication , application ; Graphene device- Carbon nanotubes fabrication ,CNT application	
		Total	**39**

Text Books:

1. James D. Plummer, Michael D. Deal, Peter B. Griffin, SILICON VLSI technology, Pearson India,2011.
2. Dieter K. Schroder, Semiconductor material and device characterization, Wiley-Blackwell; 2006.
3. Sorab K. Gandhi, “VLSI Fabrication Principles”, Wiley, Student Edition.
4. G. S. May and S. M. Sze, “Fundamentals of Semiconductor Fabrication”, Wiley, First Edition.
5. James E. Morris and Krzysztol Iniewski, “Nanoelectronic Device Applications Handbook”, CRC Press
6. Stephen A. Campbell, “The Science and Engineering of Microelectronic Fabrication”,Oxford University Press, 2nd Edition.

Assessment: Internal

Assessment Test

Assessment consists of one test on 50% syllabus.

End Semester Examination

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE2013	Testability of VLSI circuits	03	02	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE2013	Testability of VLSI circuits	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	Understand the concepts of VLSI circuits testing.
2	To provide knowledge of various modeling use for VLSI testing

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Recognize Faults and classify different fault detection in VLSI Systems design at various levels.
2	Designs develop algorithms for analysis of faults and test methodology.
3	Understand analog and mixed signal testing

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
		Pre-requisite: Digital system design, Microelectronics	
1	**Module 1**		5
		Fault Modeling and Test Generation: Importance of Testing. Testing during the VLSI Lifecycle. Challenges in the VLSI Testing: Test Generation, Fault Models. Levels of abstraction in VLSI Testing, Historical Review of VLSI Test Technology, Functional Versus Structural Testing. Levels of Fault Models, Single Stuck-at Fault. Testability measures: Controllability and Observability.	
2	**Module 2**		8
		Fault Simulation: Serial, Parallel, deductive, Concurrent, Fault Sampling. Combinational Test Generations: Random Test generation, ATPG for Combinational Circuits: D-Algorithm, PODEM. Sequential Circuit Test Generations: ATPG for single-clock synchronous circuits, Designing a Sequential ATPG, Untestable Fault Identification.	
3	**Module 3**		8
		Design for Testability: Design for Testability Basics: AdHoc Approach, Structured Approach. Scan Cell Designs. Scan Architectures. Scan Design Rules. Scan Design Flow. Special-Purpose Scan Designs. RTL Design for Testability.	
4	**Module 4**		4
		Logic Built-In Self-Test: BIST Design Rules: Unknown Source Blocking, Re-Timing. Test Pattern Generation: Exhaustive Testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing, Delay Fault Testing. Output Response Analysis. Logic BIST Architectures: BIST Architectures for Circuits with and without Scan Chains, BIST Architectures Using Register Reconfiguration. Fault Coverage Enhancement: Test Point Insertion, Mixed-Mode BIST, Hybrid BIST.	
5	**Module 5**		6
		Test Compression and Boundary Testing: Test Stimulus Compression: Code-Based Schemes, Linear-Decompression-Based Schemes. Test Response Compaction: Space Compaction, Time Compaction, Mixed Time and Space Compaction, Digital Boundary Scan (IEEE Std. 1149.1).	
6	**Module 6**		8
		Analog and Mixed-Signal Testing: Analog and Mixed-Signal Circuit Trends. Functional DSP Based Testing. Static ADC and DAC Testing Methods. Analog Fault Models. Types of Analog Testing. Analog Fault Simulation. Introduction to IDDQ Test.	
		Total	**39**

Text Books:

1. Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, “Vlsi Test Principles And Architectures” The Morgan Kaufmann, 2006.
2. Michael L. Bushnell, Vishwani D. Agrawal, “Essentials Of Electronic Testing For Digital,Memory And Mixed-Signal Vlsi Circuits”, Kap, 2002.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
4. Alexander Miczo, “Digital Logic Testing and Simulation” 2/E, A John Wiley & Sons, 2003.
5. Charles E. Stroud, “A Designer's Guide to Built-In Self-Test”, Kap. 2002.
6. Z. Navabi, “Digital System Test and Testable Design”, Springer, 2011.

Assessment: Internal
Assessment Test
Assessment consists of one test on 50% syllabus.

End Semester Examination
Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE2014	Communication buses and interfaces design	03	02	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE2014	Communication buses and interfaces design	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	To identify different serial buses such as RS232, RS485, I2C and SPI bus.
2	To understand serial communication protocols.
3	To develop different applications using communications protocols

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Select a particular serial bus suitable for a particular application.
2	Develop APIs for configuration, reading and writing data onto serial bus.
3	Design and develop peripherals that can be interfaced to desired serial bus.

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
1	**Module 1**		5
		Serial Busses - Physical interface, Data and Control signals	
2	**Module 2**		8
		features, limitations and applications of RS232, RS485, I2 C, SPI	
3	**Module 3**		8
		CAN - Architecture, Data transmission, Layers, Frame formats, applications.	
4	**Module 4**		4
		PCI e - Revisions, Configuration space, Hardware protocols, applications	
5	**Module 5**		6
		USB - Transfer types, enumeration, Descriptor types and contents, Device driver.	
6	**Module 6**		8
		Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable.	
			39
		Total	**39**

Text Books:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ", Lakeview Research, 2nd Edition.
2. Jan Axelson, "USB Complete", Penram Publications.
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press.
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x.
6. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org.

Internal Assessment: Assessment Test

Assessment consists of one test on 50% syllabus.

End Semester Examination

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE2021	VLSI architecture for signal processing	03	02	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE2021	VLSI architecture for signal processing	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	Design and optimize VLSI architectures for basic DSP algorithms.
2	Optimizing digital filters for performance.
3	Design and analyze low power DSP architectures for high performance.
4	Develop some signal processing applications using FPGA.

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Comprehension of VLSI design methodology for signal processing systems.
2	Compare different VLSI algorithms for using in a particular application.
3	Develop DSP algorithms using pipelining and parallel processing approaches.
4	Implement basic architectures for DSP using CAD tools.

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
		Pre-requisite: Digital signal processing, Advance VLSI design	
1	**Introduction**		6
		Introduction, Overview of DSP – FPGA Technology – DSP Technology requirements – Design Implementation	
2	**Fundamentals of DSP**		6
		Methods of critical path reduction, Binary Adders – Binary Multipliers – Multiply Accumulator (MAC) and sum of product (SOP) –Pipelining and parallel processing – retiming – unfolding – systolic architecture design	
3	**DSP algorithm optimization**		5
		Algorithmic strength reduction methods and recursive techniques	
4	**Filter Design**		8
		Filter Design Fast convolution-pipelined and parallel processing of recursive and adaptive filters – fast IIR filters, design.	
5	**Pipelining Filters**		8
		Design of pipelined digital filters -Designing FIR filters – Digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic – scaling and round-off noise.	
6	**DSP architecture optimization**		6
		Synchronous asynchronous pipelining and programmable DSP- Numeric strength reduction – synchronous – wave and asynchronous pipelines – low power design – programmable DSPs – DSP architectural features/alternatives for high performance and low power	
		Total	39

Text Books:

1. KeshabK.Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, John Wiley, Indian Reprint, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007. E-Resources:
3. S.Y.Kuang, H.J. White house, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1995.

Assessment: Internal

Assessment Test

Assessment consists of one test on 50% syllabus.

End Semester Examination

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE2022	Wireless Sensor Network	03	02	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Avg					
VEPE2022	Wireless Sensor Network	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	To understand the fundamentals of wireless sensor networks and its application to critical real time scenarios.
2	To study the various protocols at various layers and its differences with traditional protocols.
3	To understand the issues pertaining to sensor networks and the challenges involved in managing a sensor network

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Technical knowhow in building a WSN network.
2	Analysis of various critical parameters in deploying a WSN

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
1	**Introduction**		5
		Fundamentals of wireless communication technology, the electromagnetic spectrum radio propagation, characteristics of wireless channels, modulation techniques, multiple access techniques, wireless LANs, PANs, WANs, and MANs, Wireless Internet.	
2	**Introduction to adhoc/sensor networks**		8
		Key definitions of adhoc/ sensor networks, unique constraints and challenges, advantages of ad-hoc/sensor network, driving applications, issues in adhoc wireless networks, issues in design of sensor network, sensor network architecture, data dissemination and gathering.	
3	**MAC Protocols**		8
		Issues in designing MAC protocols for adhoc wireless networks, design goals, classification of MAC protocols, MAC protocols for sensor network, location discovery, quality, other issues, S-MAC, IEEE 802.15.4.	
4	**Routing Protocols**		4
		Issues in designing a routing protocol, classification of routing protocols, table-driven, on-demand, hybrid, flooding, hierarchical, and power aware routing protocols.	
5	**QoS and Energy Management**		6
		Issues and Challenges in providing QoS, classifications, MAC, network layer solutions, QoS frameworks, need for energy management, classification, battery, transmission power, and system power management schemes.	
6	**Sensor Network Platforms And Tools**		8
		Sensor Node Hardware – Berkeley Motes, Programming Challenges, Node-level software platforms – TinyOS, nesC, CONTIKIOS, Node-level Simulators – NS2 and its extension to sensor networks, COOJA, TOSSIM, Programming beyond individual nodes – State centric programming.	
		Total	39

Text Books:

1. C. Siva Ram Murthy, and B. S. Manoj, "AdHoc Wireless networks ", Pearson Education -
2. Feng Zhao and Leonides Guibas, "Wireless sensor networks ", Elsevier publication - 2004.

Assessment: Internal Assessment Test

Assessment consists of one test on 50% syllabus.

End Semester Examination

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE2023	Device Drivers	03	02	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Total					
VEPE2023	Device Drivers	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	
2	
3	

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	
2	
3	
4	
5	
6	

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
1	**Module 1**		5
		Introduction to operating system, Introduction to Linux Basics, commands, file system , kernel and introduction to Android,	
2	**Module 2**		8
		Process Synchronization ,Semaphores, Message Passing, Mailboxes and debugging	
3	**Module 3**		8
		Module programming/ Shell programming / Character Device Driver	
4	**Module 4**		4
		Timing and Interrupts	
5	**Module 5**		6
		Device Driver Programming as applicable to Linux/ Android/ Windows	
6	**Module 6**		8
		Parallel/ Serial Port Driver/ Block /USB /NETWORK/ PCI/ Drivers, tty Subsystem	
			39

Text Books:

Internal Assessment:
Assessment Test
Assessment consists of one test on 50% syllabus.

End Semester Examination
Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.

Course Code	Course Name	Theory	Practical	Tutorial	Theory	Practical/ Oral	Tutorial	Total
VEPE2024	Neural networks and Machine learning algorithms	03	02	--	03	01	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Mid Term	CA	Total					
VEPE2024	Neural networks and Machine learning algorithms	20	20	40	60	25	--	--	125

Sr. No.	Course Objectives
The course aims:	
1	Know neural networks
2	To implement Machine learning applications

Sr. No.	Course Outcomes
On successful completion, of course, learner/student will be able to:	
1	Grasp and develop machine learning algorithms namely linear, logistic and multivariate regression
2	Design and implement machine learning solutions to classification and clustering problems
3	Evaluate and interpret the results of the machine learning algorithms

DETAILED SYLLABUS

Module No.	Unit No.	Topics	Hrs.
1	**Module 1**		5
		Fundamentals and definitions; Perceptron, backpropagation and counter propagation Networks; Introduction to Perceptron and SVM, Neural Networks: Introduction, Early Models, Perceptron Learning, Back-propagation, Initialization of neural network, Training and Validation, Parameter Estimation	
2	**Module 2**		8
		Statistical methods for network training; Hopfield nets; Associative memories; Optical neural networks	
3	**Module 3**		8
		Regression: Linear Regression, Multivariate Regression, Subset Selection, Shrinkage Methods, Principal Component Regression, Logistic Regression, Partial Least Squares Classification: Linear Classification, LDA	
4	**Decision Tree**		4
		Stopping Criterion and Pruning, Loss function, Categorical Attributes, Multiway Splits, Missing values, Instability, Regression Trees. Bootstrapping and Cross Validation, Class Evaluation, Measures, ROC curve, MDL, Ensemble methods, Committee Machines and Stacking.	
5	**Module 5**		6
		Gradient Boosting, Random Forests, Multi-class Classification, Naïve Bayes, Bayesian Networks, Undirected Graphical Models, HMM, Variable elimination, Belief Propagation, Partitional clustering, Hierarchical Clustering, Birch Algorithm, CURE Algorithm, Density- Based Clustering, Gaussian Mixture Models, Expectation Maximization, Learning Theory, Re-enforcement Learning	
6	**Module 6**		8
		Applications of neural networks in speech processing, computer networks and visual processing.	
			39

Text Books:

1. Ethem Alpaydin, “Introduction to Machine Learning”, PHI, 2005
2. Bishop Christopher, “Neural Networks for Pattern Recognition”, New York, NY: Oxford University Press, ISBN: 9780198538646
3. Mitchell Tom, “Machine learning”, New York, NY: McGraw-Hill, ISBN:9780070428072
4. Hastie, T. R. Tibshirani, and J. G. Friedman, “The Elements of Statistical Learning: Data VLSI & ES Page 10 Mining, Inference and Prediction”, New York, NY: Springer, ISBN:9780387952840

Internal Assessment Test

Assessment consists of one test on 50% syllabus.

End Semester Examination

Some guidelines for setting the question papers are as, five questions to be set each of 20 marks, any three out of five with no internal choice.