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Common Mode Voltage Removal using New Balancing Technique for Extraction of Low Level Differential Signals Embedded in Large Common Mode Voltages

Nilima Warke, J. M. Nair, P. P. Vaidya

Abstract*: The paper proposes a method based on new principle for removal of common mode voltages (CMVs) present in the differential signals [#]. These CMVs can be reduced nearly to zero without using any components with tight tolerances which is achieved using a new balancing technique. It is proved that the performance of the circuit depends only on the ratios and not on the individual values of the resistors because of which the performance of the circuit is not affected over the wide range of temperature. The circuit based on this principle was designed, constructed, tested and results are reported in this paper. Unlike the conventional techniques which use filters for removal of the common mode signals in specific band of the frequencies, the method reported here removes common mode signals of all known and unknown frequencies. Using this method, it is possible to extract very low values of the differential signals in the range of few microvolts where common mode voltages can be as high as few volts. It is possible to improve the effective common mode rejection ratio (CMRR) of any differential amplifier by a factor of more than 10^3 to 10^4 with this method.

***Keywords*: Balancing technique, common-mode rejection ratio, common mode voltage removal, differential amplifier, instrumentation amplifier.**

I. INTRODUCTION

In many applications, it is required to amplify the extremely weak differential signals (AC+DC) in presence of large common-mode signals [1]. For example, in biomedical applications, the actual differential ECG signal that appears between the electrodes in any lead configuration is generally limited to ±5 mV in magnitude and 0.05 Hz to 150 Hz in frequency with an additional DC offset which can be as high as 300 mV due to the skin-electrode interface. In addition to these two signals, the human body can pick up large interference signals from power lines, fluorescent lights, and so forth [2]. This interference can appear as either a normal-mode signal or a common-mode signal as shown in Fig. 1.In general principle of amplification of differential signal is also associated with amplification of CMV signal by very
small factor known as common mode gain [3] as shown in Fig. 2 where, Vid =(Va –Vb)- which is differential voltage to be measured.

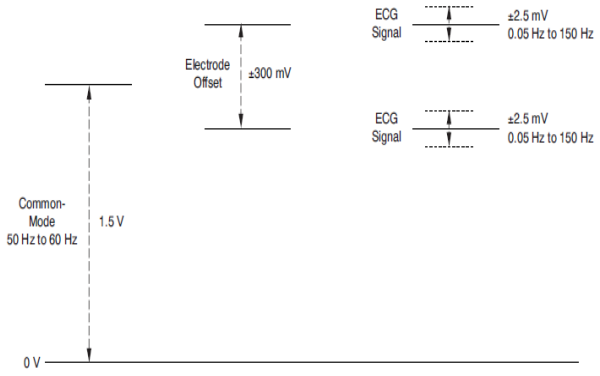

Fig. 1: ECG signal characteristics [2]

Here,

Vcm- Common mode voltage,
Ad – Differential gain
Acm – Common-mode gain
Vo- output of the amplifier.

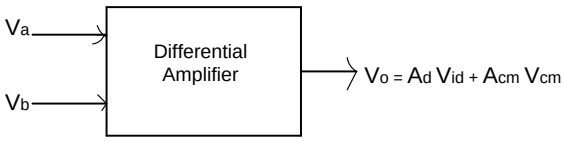

Fig. 2: Typical Differential amplifier configuration

There are several techniques which are utilised for reduction of CMV due to power line interference of known frequency using driven right leg circuit, notch filter, adaptive filters and Digital FIR filters as reported in [4]-[9]. These methods are effective for the narrower frequency band to get tolerable amplitude and phase distortion. However, there are certain applications where it is not possible to reduce the CMV as given in the following example.

In many sensors processing applications very small changes in resistances are required to be measured using bridge configuration which results into low differential voltage in presence of large CMV [10].

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This CMV can be as large as 5V for a supply voltage of 10V for the bridge configuration as shown in Fig. 3.

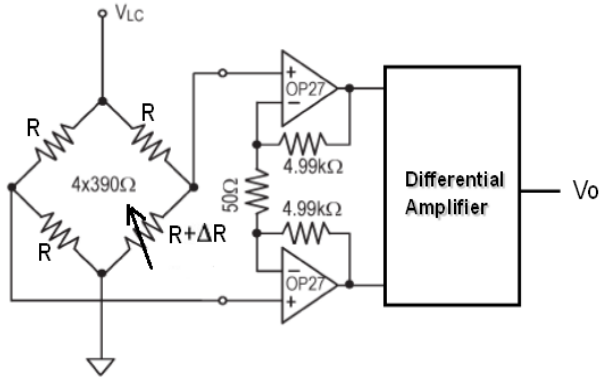

Fig. 3: Signal conditioning of Sensor output

The differential voltage will be nearly 5µV when change in R is very small as compared to R i.e nearly R X 10^{-6}. In conventional instrumentation amplifier (IA), the CMRR is generally available in the range of 10^5 to 10^6. For such application, with differential gain of 200, output of IA corresponding to differential voltage will be 1mV and common mode output voltage of IA will be in the range of 1mV to 10mV. It is obvious that the effect of CMV is much larger as compared to differential voltage and because of which it is not possible to measure such extremely small changes in R under this condition.

Moreover here, since the frequency of the common mode signal and the differential signal being the same, the common mode signal cannot be removed using any filtering technique.

The conventional way of addressing this problem is to improve CMRR to adequately high value in the range of 10^8 to 10^9. However, this requires design of intricate circuits of IA and conventional IAs cannot be used for such applications where small differential voltages are required to be amplified in presence of large CMV.

Here, a new method of reducing the CMV present in the signal to a very low value (nearly equal to zero) using new balancing technique has been proposed. Using this method, conventional IAs can be used for such applications and effective CMRR can be improved beyond 10^9 particularly when large values of CMVs are present.

II. PROPOSED SYSTEM

A. Proposition of Principle:

Va and Vb are two input signals having CMVs as shown in Fig. 4.The aim of this work is to reduce the CMV to zero by generating new balanced outputs Vx and Vy of equal amplitude and opposite polarity such that the CMV is reduced to zero by keeping differential voltage same. Thus only differential signalscan be amplified by any normal differential amplifier without having any effect of its CMRR.

The schematic diagram of CMV removal by using this new balancing technique is as shown in Fig. 5.

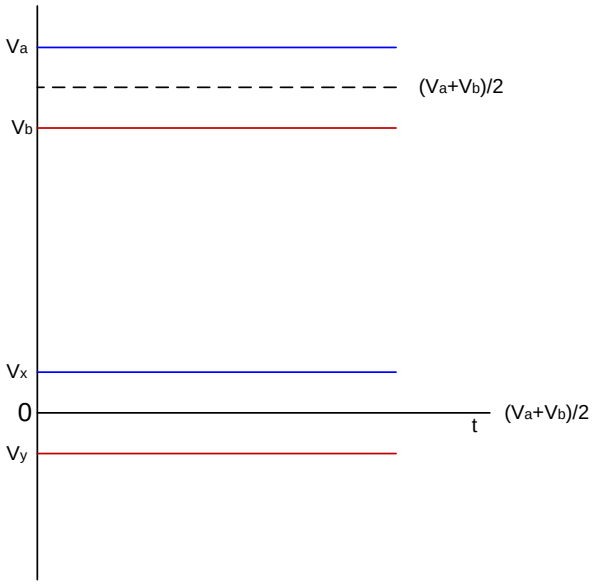

Fig. 4: Principle of common mode voltage removal

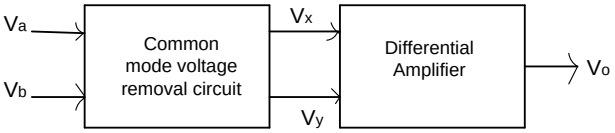

Fig. 5: Schematic diagram of CMV removal by generating

Balanced output voltages Vx ad Vy

Here,

Common mode voltage Vcm = (Va + Vb)/2

Differential voltage Vid = (Va – Vb)

Let Vx and Vy two voltages to be generated such that ---

(Vx-Vy) = (Va-Vb) ---(1)

(Vx +Vy)/2 = 0 ---- (2)

From eq(2) Vx = -Vy ---(3)

Substitute (3) in (1) which gives—

Vy = (Vb-Va) /2 ----(4)

Similarly, Vx = (Va-Vb) /2 ---(5)

Eq (5) can be written as—

Vx = Va/2 + (Va-Vb)/2 - Va/2

Vx = Va – (Va+Vb)/2------(6)

Similarly,

Vy = Vb – (Va+Vb)/2 -----(7)

Now, from (6) and (7)

(Vx-Vy) = (Va-Vb) ---(8)

and (Vx +Vy)/2 = 0---(9)

From Eq (8) and (9), it can be observed that differential voltage (Vx-Vy) is same as the original differential voltage (Va-Vb) but common mode (Vx + Vy)/2 is reduced to zero.

One method using the conventional circuits for generation of Vx and Vy is as shown in Fig. 6.

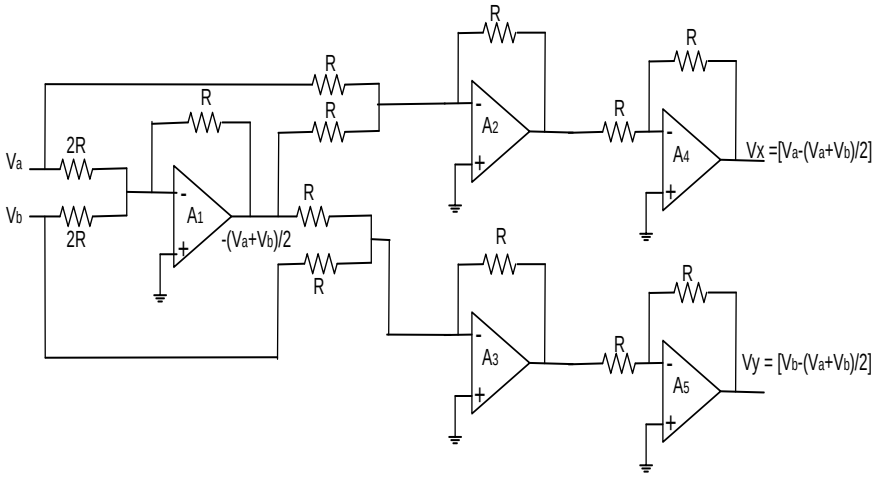

Fig. 6: Reduction of CMV using the conventional circuit

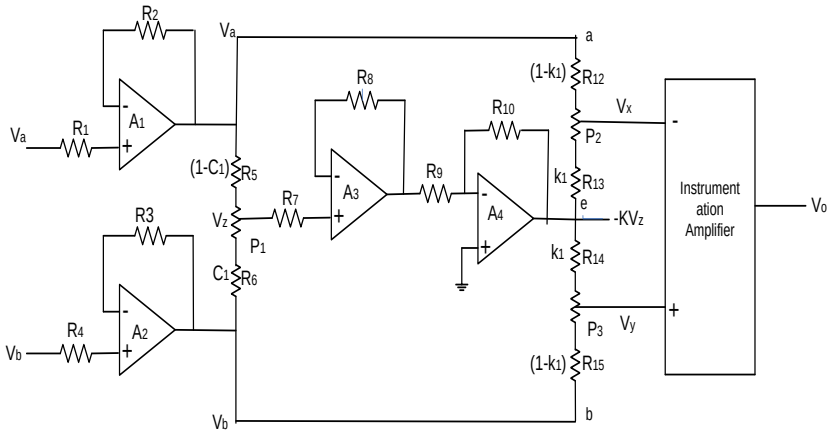

Fig. 7: Proposed circuit of common mode voltage removal

In Fig. 6, (Va+Vb)/2 is generated using summing amplifier A_1 and input resistances of 2R and feedback resistor R. Then this voltage (Va+Vb)/2 is subtracted from Va and Vb respectively using summation circuit consisting of op-amp A_2 and A_3 respectively. These signals are further inverted by unity gain inverters using op-amp A_4 and A_5 to generate final voltages of Vx and Vy.

Here, if the resistances with tolerance of +/- 0.1% are used, then it is possible that 0.1% of CMV appears as a differential voltage at the output i.e in Vx and Vy. So for CMV of 5V, the error in the differential output voltage can be as large as 5mV. Hence this conventional circuit cannot be used for reduction of such large values of common mode voltages. Therefore, to make circuit independent of component tolerances, a new method is proposed here.

The method proposed as shown in Fig.7 utilises a new balancing technique which totally removes the common mode signals. The circuit is designed without using tight tolerance resistors to remove the CMV. Thus only differential signals are present which can be amplified by any normal differential amplifier without any effect of its CMRR.

B. Description of the Proposed Circuit:

Here Va and Vb are applied as inputs to buffers made by using op-amps A_1 and A_2 respectively. The outputs of these buffers are given to chain of resistors consisting of R_5 and R_6. The maximum reduction in CMV is obtained when $R_5 = R_6$ for which the potentiometer P_1 has been provided. However, this adjustment is not critical for CMV reduction as it will be proved in the mathematical analysis of the circuit. The voltage Vz obtained at the tap of P_1 is inverted using a buffer amplifier A_3 and inverting amplifier A_4. The output of A_4 is –kVz. Here, k is gain of the inverting amplifier which will be equal to unity when R_9 and R_{10} are equal. This output is applied across the two chains of the resistors First chain consists of R_{12} , P_2 and R_{13} and second chain consists of R_{14}, P3 and R_{15} as shown in Fig.7.

During the calibration, P_2 and P_3 are adjusted to get a null condition. The output voltage Vx and Vy generated by this circuit resulted into a differential voltage which is half of the original one. However, CMV can be reduced to zero thereby improving CMRR by a factor which is more than 1000 as explained further.

As mentioned, the best results are obtained when R_5 and R_6 are equal but since the equal values of resistors may not be available, a potentiometer P_1 is adjusted for this purpose. However, this adjustment may not be perfect. To account for this effect, a factor C_1 has been introduced such that C_1 is equal to $(R_6 /(R_5 +R_6))$ and $(1-C_1) = (R_5 /(R_5 +R_6))$. For ideal adjustment, C_1 should be exactly half.

III. MATHEMATICAL ANALYSIS

To establish the balanced condition i.e Vx = Vy =0, following procedure is followed. First, a null condition is established for Va = Vb for which the same voltage is applied at both the inputs. Under this condition, the voltage at point 'e' of Fig. 7 is equal to –kVa. The null conditions are established by adjusting potentiometers P_2 and P_3 to get Vx =Vy = 0. Equivalent circuit for this condition is as shown in Fig. 8 which is clearly a bridge circuit for which the balanced condition is being adjusted.

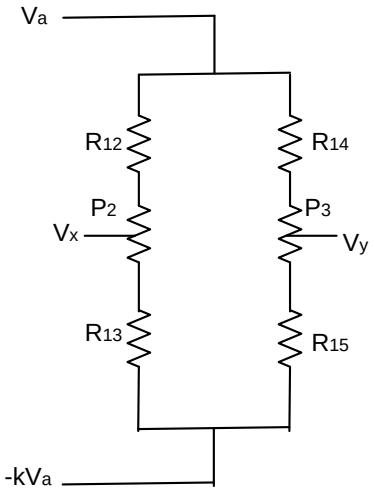

Fig. 8: Equivalent diagram of resistor chains when Common input Va is applied

The resistors R_{12} and R_{13} include the resistance values of the adjusted potentiometer P_2 and R_{14} and R_{15} include the adjusted value of potentiometer P_3.

By superposition theorem,

$Vx = [R_{12}/(R_{12} + R_{13})] [-kVa] + [R_{13}/(R_{12} + R_{13})] [Va]$ ----------(11)

$Vy = [R_{14}/(R_{14} + R_{15})][-kVa]+[R_{15}/(R_{14}+R_{15})][Va]$ ----------(12)

At balanced condition Vx =Vy =0

Therefore the bridge will be balanced at

$(R_{13}/ R_{12}) = (R_{15}/ R_{14})$

Now, Let $[R_{13}/(R_{12} + R_{13})] = k_1$

so $[R_{12}/(R_{12} + R_{13})] = (1-k_1)$

Eq (11) can be written for balanced condition i.e Vx = 0 as ---

$Vx = (1-k_1)\ (-kVa) + k_1\ (Va) = 0$

So $k_1 = k / (k + 1)$ ----------(13)

When Va and Vb are applied at the inputs, the equivalent diagrm is as shown in Fig. 9. Under this condition, the voltage at point 'e' in Fig. 7 is –kVz where Vz is the voltage at the input to the buffer made by using op-amp A_3. This voltage Vz can be adjusted to zero when Va = -Vb for which Vz should be equal to zero by adjusting potentiometer P_1. Under this condition, $R_5 = R_6$. However, it may not be possible to adjust the pot value P1 for exact null condition in which case $Vz = C_1\ Va + (1-C_1)\ Vb$. Hence Vx and Vy are given by following Eq (14) and (15).

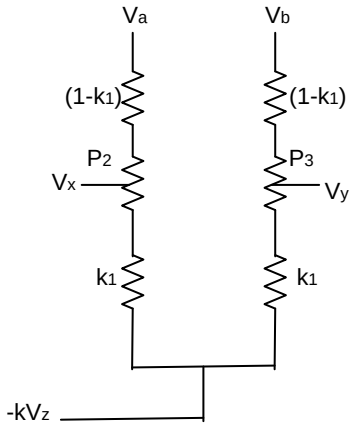

Fig. 9: Equivalent diagram wnen Va and Vb applied as inputs to the resistor chains

$Vx = k_1\ Va + (1-k_1)\ (-kVz)$ ----------(14)

$Vy = k_1\ Vb + (1-k_1)\ (-kVz)$ ----------(15)

Hence,

$[Vx + Vy] = [k_1Va + (1-k_1)\ (-kVz)] + [k_1\ Vb + (1-k_1)\ (-kVz)]$

$[Vx + Vy] = k_1\ (Va + Vb) + (1-k_1)\ (-2kVz)$

Substituting k_1 from equation (13) –

$[Vx + Vy] = k_1\ (Va + Vb) + [1-(k/(k+ 1))] (-2kVz)$

$= (k /(k +1)) (Va+Vb) – (2kVz/(k+1))$

$= (k /(k +1)) (Va + Vb – 2Vz)$ -----(16)

Substituting the value of Vz,

$[Vx + Vy] = (k /(k +1)) [(Va + Vb)– 2(C_1\ Va + (1-C_1)\ Vb)]$

The common mode voltage $[Vx + Vy]/2$ is--

$[Vx + Vy]/2 = [(k/(k + 1))\ (1-2C_1)\ (Va-Vb)]/2$ ----(17)

Similarly, the differential voltage [Vx - Vy] is---

$[Vx - Vy] = (k/(k + 1))\ (Va – Vb)$ -----(18)

In ideal case when the potentiometer settings are adjusted perfectly, k =1 and C_1=1/2. Eq (17) and (18) reduced to the following equations:

$[Vx + Vy]/2 = 0$ and

$[Vx - Vy] = (Va – Vb) /2$

From the above case, it is clear that CMV is reduced to zero and differential voltage is reduced to half. Hence effective CMRR is improved significantly. However, in case the adjustments of the potentiometers are not perfect as indicated by Eq (17), the CMV $[Vx + Vy]/2$ is proportional to differential voltage (Vx-Vy) as given by the following equation --

$[Vx + Vy]/2 = C\ (Vx-Vy)$ ------- (19)

Where $C = [(k/(k + 1))\ (1-2C_1)]/2$ ------(20)

Eq (19) indicates that the CMV is converted to the differential voltage irrespective of value of C_1 and k. Hence the effect of CMV is fully neutralized. This point can be further elaborated under extreme condition of potentiometer adjustments i.e for $C_1 = 1$ and $C_1 = 0$ as---

Case 1) if C_1=1 then Vz = Va and

Vx = 0 and Vy = (Vb – Va) /2

Vid = (Vx- Vy) = (k/(k + 1)) (Va – Vb)

Vcm = [Vx + Vy]/2 = - (k/(k + 1))/2 (Vx-Vy) ----(21)

Similarly

Case 2) if C_1=0 then Vz = Vb and

Vy = 0 and Vx = (Va – Vb) /2

Vid = (Vx- Vy) = (k/(k + 1)) (Va – Vb)

Vcm = [Vx + Vy]/2 = (k/(k + 1))/2 (Vx-Vy) ----(22)

From the above derivations, it is clear that CMV is converted to a factor which is proportional to the differential voltage and hence the effect of CMV is totally neutralized. The values of CMV and differential voltage available from this circuit depend only upon the ratios of k and c and not on the individual value of the resistor used for this purpose. These ratios will remain constant over a wide temperature range when resistors have low temperature coefficient of tracking.

IV. RESULTS

The CMV removal circuit as shown in Fig. 7 was designed, constructed and tested for various common mode and differential signals. The circuit was constructed using 1% tolerance metal film resistors and op-amp type LF356 of Texas Instruments. The outputs available from this circuit were given as inputs to INA which was constructed using IC type AD620 of Analog Devices to give the gain of 4.

Signals Va and Vb were generated having different values of differential voltages and CMVs and then applied as inputs to the proposed circuit. Typical Vcm and Vid is as shown in Fig 10. The composite signal Va was generated by addition of Vcm and Vid whereas the Vcm signal itself was used as Vb as shown in Fig. 11. The waveforms of Vx and Vy obtained as output of this circuit are as given in Fig. 12 and the final output Vo is as shown in Fig. 13.

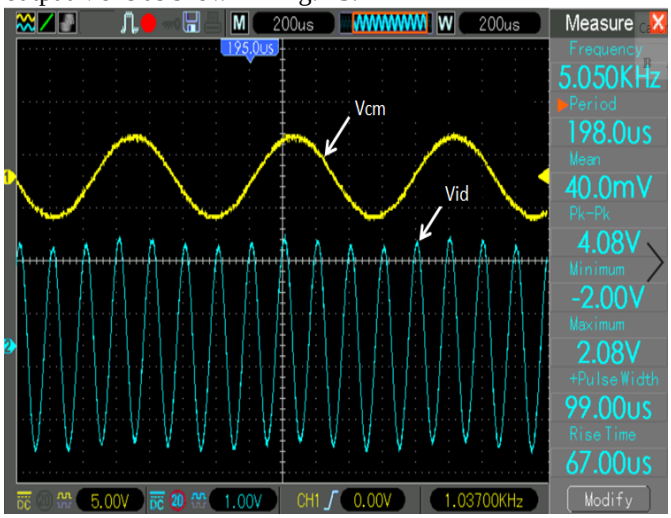

Fig 10: Waveforms of Vcm and Vid

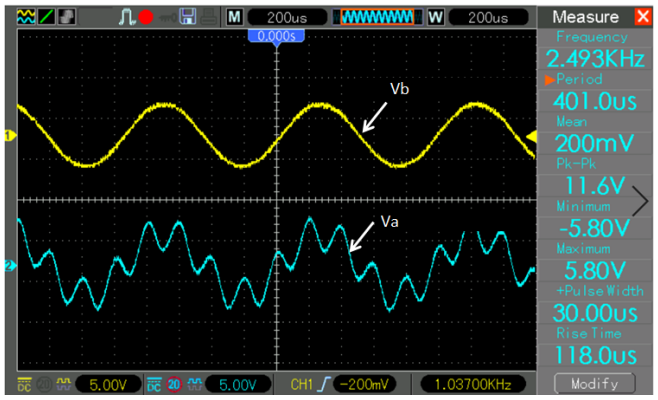

Fig 11: Waveforms at point Vb and Va

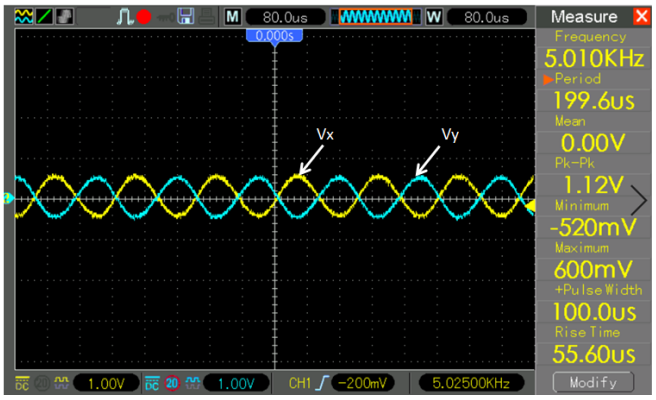

Fig 12: Waveforms observed at point Vx and Vy

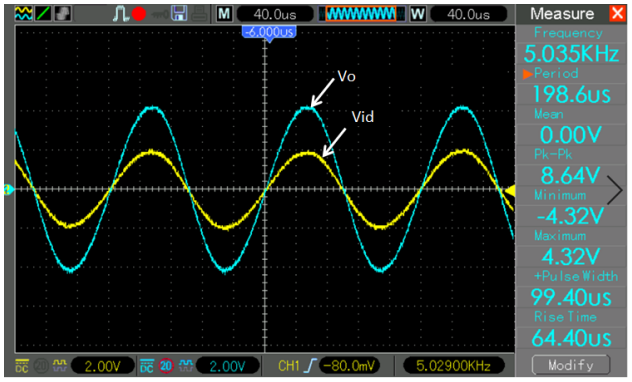

Fig 13: Waveforms observed at point Vid and Vo

Common mode Voltage Performance:

The circuit performance for CMV was tested for common mode sinusoidal input voltages with a peak to peak value as 4V and 8V at different frequencies. The corresponding outputs were measured and plotted as shown in Fig. 14. It can be observed from these graphs that the reduction in CMV depends upon the frequency and the reduction factor decreases with frequency. This behavior is due to the finite phase shift created by op-amp A_4 used as inverting amplifier whose performance depends upon the frequency. In this circuit op-amp type LF356 has been used for this purpose. The op-amp with wide bandwidth can be used to improve the performance at high frequencies.

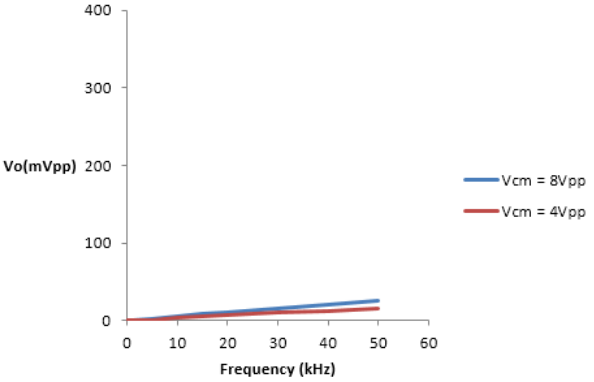

Fig. 14: Common mode Voltage performance of the proposed CMV removal circuit

Differential Voltage Performance:

The differential voltage performance of the circuit was also tested at various frequencies from 1Hz to 100kHz for common mode sinusoidal signal of 55Hz with peak to peak value of 8V as shown in Fig. 15.

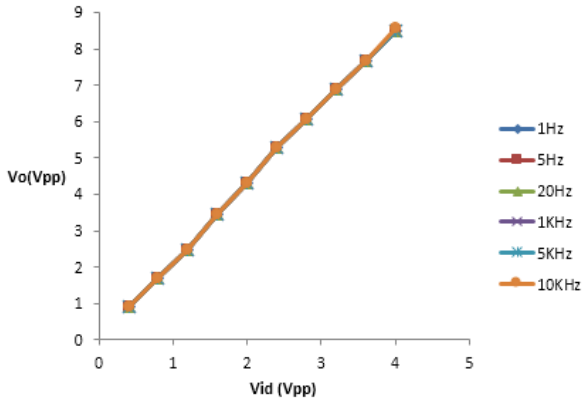

Fig. 15: Differential Voltage performance of the proposed CMV removal circuit

The results which have been plotted as given in Fig. 14 and 15 clearly ascertain that the CMV signal is scaled down by a factor of more than 10,000 without affecting the frequency response for differential signal.

V. CONCLUSION

The paper proposes a method based on new balancing principle for extraction of low level differential signals in presence of large common mode signals. Low level differential signals having amplitudes of as small as few microvolts can be extracted from common mode signals which can be as large as few volts. The common mode voltage is reduced to zero under perfectly balanced condition. The circuit was constructed using this method without use of components with tight tolerances. The results obtained by testing of the circuit show that it is possible to obtain reduction in common mode voltages by a factor which can be as high as 20000 whereas differential voltage is reduced only by factor of two. Use of this circuit at input of any instrumentation amplifier can improve effective CMRR by a factor of more than 1000. The balancing condition does not depend upon values of individual resistors but on their ratios. Because of this it is possible to use resistors with low temperature coefficients of tracking so that the circuit performance is not degraded over wide range of temperature.

ACKNOWLEDGMENT

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